



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

Wonju Cho, et al.

Application No.: 10/749,749

Filed: December 30, 2003

For: MOSFET DEVICE WITH NANOSCALE

CHANNEL AND METHOD OF MANUFACTURING THE SAME

Art Group: 2818

Examiner: Dang, Phuc T

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted before the mailing of a final Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The references were cited in a Search Report dated January 17, 2005 (copy enclosed herewith) in a counterpart Korean application, which was forwarded to Applicant's Representative in a communication dated January 18, 2005.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOPOFF, TAYLOR & ZAFMAN LLP

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Kumiko Alexander

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Sheet 1 of 2

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		Complete if Known
	Application Number	10/749,749
	Filing Date	December 30, 2003
	First Named Inventor	Wonju Cho
	Art Unit	2818
_	Examiner Name	Dang, Phuc T
	Attorney Docket Number	2013P148

	U.S. PATENT DOCUMENTS				
		Document Number	Publication Date		Pages Columns Lines Where
Examiner Initials*	Cite No.1	Number - Kind Code ² (if known)	or feeua Data	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-6452229 B1	09-17-2002	Krivokapic	
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	FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No.1	Foreign Patent Document		Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	76
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY			10
		10-1994-030879	10-01-1998	LG Semiconductor Co. Ltd.		
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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08A (08-03) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 08/11/2003.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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2 2 of Sheet

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Art Unit	2818
Examiner Name	Dang, Phuc T
Attorney Docket Number	2013P148

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²	
		A. CHATTERJEE, et al. "Sub-100nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process," Semiconductor Process and Device Center, 1997 IEEE, pps. 821-824		
		H-H. VUONG, "Design of 25-nm SALVO PMOS Devices," IEEE Electron Device Letters, Vol. 21, No. 5, May 2000, pps. 248-250.		

Examiner	Date		
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